

Notice of References Cited	Application/Control No. 10/711,493		Applicant(s)/Patent Under Reexamination KAPOOR ET AL.	
	Examiner Russell Frejd		Art Unit 2128	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,152,216	12-2006	Kapoor et al.	716/4
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	MUNCH et al., M. Automating RT-Level Operand Isolation to Minimize Power Consumption in Datapaths, Proceedings of the conference on Design, automation and test in Europe DATE '00, January 2000, pp. 624-31.
	V	ZARRINEH et al., K. System-on-Chip testability Using LSSD Scan Structures, IEEE Design & Test of Computers, Vol. 18, May-June 2001, pp. 83-97.
	W	MAMIDIPIKA et al., M. IDAP: A Tool for High-Level Power Estimation of Custom Array Structures, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 23, No. 9, September 2004, pp. 1361-9.
	X	PARK et al., Y.-H. Embedded DRAM (eDRAM) Power-Energy Estimation for System-on-a-Chip (SoC) Applications, 7th Asia and South Pacific International Conference on VLSI Design, January 2002, pp. 625-30.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.